The opinion in support of the decision being
entered today was <u>not</u> written for publication
and is <u>not</u> binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

<u>Ex parte</u> KARL-EUGEN KROELL,
JURGEN PILLE,
and HELMUT SCHETTLER

Appeal No. 2006-2382
Application 09/902,140[1]
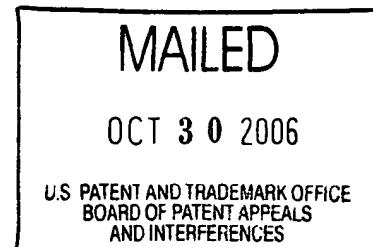
ON BRIEF

Before BARRETT, LEE, and MEDLEY, <u>Administrative Patent Judges</u>.

BARRETT, <u>Administrative Patent Judge</u>.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1, 2, 5-8, 13, and 14.

We reverse.

BACKGROUND

The invention relates to a method and system for simulating hardware circuits, which is particularly useful for Silicon-on-Insulator (SOI) hardware circuits. SOI-type hardware states,

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[1] Application for patent filed July 10, 2001, entitled "Automatic Check for Cyclic Operating Conditions for SOI Circuit Simulation."

- 1 -

e.g., the voltages occurring at any node of a circuit, are dependent upon the history during which the hardware has been operated. Therefore, cyclic operating conditions have to be investigated and simulated for circuits in SOI technology. A "functional cycle" represents a defined operating interval having a start time and a stop time in which, at both times, the input voltages are the same. The invention checks if the voltage at CYCLE START matches its voltage at CYCLE STOP under static (DC) simulation conditions. If not, an indication is obtained which helps to automatically localize and manually correct voltage mismatches that are caused by non-cyclic input voltage waveforms. Example of mismatches between CYCLE START and CYCLE STOP are described in the specification, pages 10-11.

Claim 1 is reproduced below.

1. A method for simulating hardware circuits during which voltages are calculated at a plurality of circuit nodes, comprising the steps of:

(a) carrying out a first DC-simulation run at the beginning of a functional cycle,

(b) carrying out a second DC-simulation run at the end of said cycle,

(c) comparing simulated values from both runs at respective circuit nodes, and

(d) storing mismatch information about static error afflicted nodes at which the calculated values differ by more than a predetermined first threshold value.

THE REFERENCES

The examiner relies on the following references:

Wong (Wong '643)   4,918,643   April 17, 1990
Sakamoto   6,063,130   May 16, 2000
Joshi et al. (Joshi)   6,442,735   August 27, 2002
                                        (filed March 15, 2000)

Billy K.H. Wong and Henry Chung, Accelerated Steady-State Analysis Technique for PWM DC/DC Switching Regulators, IEEE Industrial Electronics, Control and Instrumentation, 1997, IECON 97, 23rd International Conference on New Orleans, LA, USA, 9-14 Nov. 1997, New York, NY, pp. 759-764 (cite from search report in PCT/EP 01/08780) (hereinafter Wong IEEE).

THE REJECTIONS

The obviousness-type double patenting rejection has been withdrawn (answer, p. 3).

Claims 1, 5, 7, and 13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Wong '643 or Wong IEEE.

Claims 1, 2, 5-8, 13, and 14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Joshi.

Claims 1, 2, 5-8, 13, and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakamoto and either of Wong '643 or Wong IEEE.

We refer to the final rejection (pages referred to as "FR__") entered September 17, 2003, and the examiner's answer (pages referred to as "EA__") entered April 20, 2004, for a statement of the examiner's rejection, and to the brief (pages referred to as "Br__") received February 10, 2004, for a statement of appellants' arguments thereagainst.

DISCUSSION

Anticipation

Wong '643

Appellants argue that Wong '643 does not do a DC simulation of end of cycle conditions and does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop (Br5). Thus, we look to see what the examiner relies upon to meet these specific limitations.

The examiner interpreted "that static error corresponds to the DC-simulation and that dynamic error corresponds to the transient analysis" (EA3). The examiner states the issue as follows (EA4): "Does a prior art teaching of a determination of whether a simulation of a circuit has *converged* on a *steady state* behavior read on the claimed invention." (Note, it is always the claims that are read on the prior art, not vice versa.) The examiner finds that Wong '643 discloses a method of accelerating the pace at which circuit simulators are able to converge to a steady state solution and, in particular, Wong '643 discloses DC analysis with error detection and correction at Figs. 2-4 and 13, and column 2, lines 7-33; column 3, line 23 to column 5, line 14; and columns 11-12 (EA4). It is stated that appellants have not addressed the specific sections of Wong '643 relied upon in the rejection (EA8).

Claim 1 is simple and straightforward and we expect the rejection to clearly point out where Wong '643 discloses each step. Instead, the examiner has rephrased the issue as one of determining convergence to a steady state behavior without explaining how such determination would satisfy the claim language of "(a) carrying out a first DC-simulation run at the beginning of a functional cycle, (b) carrying out a second DC-simulation run at the end of said cycle, (c) comparing simulated values from both runs at respective circuit nodes." The examiner states (EA10): "To determine whether circuit behavior has converged to a steady-state *requires a comparison of the same circuit node* over time (different DC conditions cause[d] by the iterative charging or discharging of a circuit element in the previous iteration in the circuit simulation[)]." However, this does not explain the correspondence to the limitations of "(a) carrying out a first DC-simulation run at the beginning of a functional cycle," and "(b) carrying out a second DC-simulation run at the end of said cycle." "Steady state" and "iterations" do not imply DC conditions. Nor has the examiner pointed out what corresponds to the "functional cycle." The examiner interprets "that static error corresponds to the DC-simulation" (EA3) without defining "static error" and without pointing out where Wong '643 discusses static error, and we do not find the word "static" mentioned anywhere in Wong '643.

Although the specification discusses that conventional simulation requires simulation of many cycles until a steady state is approached (convergence) and that iterative methods are much more efficient (specification, p. 3, lines 4-14), and while Wong '643 mentions "steady state," "iterative" techniques, and "errors," this is a discussion of the prior art and not the claimed invention.

Wong '643 discloses a method for more quickly arriving at the steady state of closed-loop self-regulated or periodically driven piecewise-linear systems. The system is switched between various topologies in a switching cycle (e.g., col. 1, lines 50-52; col. 3, lines 18-22). The state of the system is represented by state variables that collectively form a state vector. The process iteratively repeats until the initial state vector and the final state vector are within a user specified tolerance (abstract). The examiner has not clearly explained, nor do we find, how the process in Wong '643 involves carrying out first and second DC-simulation runs and then comparing the simulated values from the runs. The examiner has failed to make out a prima facie case of anticipation. The rejection of claims 1, 5, 7, and 13 is reversed.

Wong IEEE

Appellants argue that Wong IEEE does not do a DC simulation of end of cycle conditions and does not store mismatch information between two DC simulations corresponding to cycle start and cycle stop (Br5). Thus, we look to see what the examiner relies upon to meet these specific limitations.

The examiner again operates under the assumption that the issue is whether the claimed invention reads on the prior art teaching of determining whether a circuit has converged on a steady state behavior. The examiner finds that Wong IEEE discloses an iterative technique for steady-state analysis of switching regulators using two iteration loops and, in particular, Wong IEEE discloses DC analysis with error detection and correction at Figs. 2-3 and the corresponding text (EA5). It is stated that appellants have not addressed the specific sections of Wong IEEE relied upon in the rejection (EA8).

We incorporate by reference our discussion of the examiner's rejection over Wong '643. As with the rejection over Wong '643, the examiner has not pointed out how the claim steps correspond to the teachings of Wong IEEE. Wong IEEE is directed to an iterative technique for computing the steady-state solution of PWM (pulse width modulation) DC/DC switching regulators (p. 759). We do not find any disclosure of performing a DC simulation at the beginning and end of a

functional cycle, or comparing the simulated values. The
examiner has not made out a prima facie case of anticipation.
The rejection of claims 1, 5, 7, and 13 is reversed.

Joshi

Appellants note that Joshi discloses an SOI circuit
simulation method where "DC analysis" is performed prior to
transient response simulation and the DC analysis appears to be
an assessment relative to an initial DC condition, but argue
that Joshi does not disclose <u>comparing</u> device response to two
different DC conditions or storing any information based on such
a comparison (Br5-6).

The examiner generally describes the teachings of Joshi
(EA5; EA9), but does not explain where each claim step is found
in Joshi. Joshi discloses performing an initial DC analysis,
step 1240 in Fig. 2, before performing a transient analysis,
step 1260 in Fig. 2, but does not disclose performing a second
DC-simulation run at the end of a cycle or comparing the
simulated values to determine mismatch information. The
examiner has not made out a prima facie case of anticipation.
The rejection of claims 1, 2, 5-8, 13, and 14 is reversed.

Obviousness

The examiner finds that Sakamoto discloses a steady-state
simulation followed by a transient simulation, but that it does

not disclose checking the simulations for errors and then
correcting the errors (FR8). The examiner finds that Wong '643
and Wong IEEE disclose checking simulations to ensure accuracy
and correcting simulations when the error is significant (FR8).
The examiner concludes that it would have been obvious to modify
Sakamoto in view of Wong '643 or Wong IEEE because
"[s]teady-state and transient simulations are not very useful or
realistic if they are not accurate" (FR10).

Appellants argue that Sakamoto, at best, teaches a DC
analysis of the cycle start condition and does not disclose or
suggest comparing device response to two different DC
conditions, not storing any information based on such a
comparison (Br6). It is argued that Sakamoto does not disclose
or suggest performing corrections based on such comparison of
conditions prior to transient analysis (Br6) and that neither
Wong reference would lead one skilled in the art to perform the
comparison of DC simulations and manual corrections prior to
transient analysis in response to such a comparison (Br7).

The examiner responds that appellants are relying on the
same arguments as for the § 102 rejections and are not
persuasive for the same reasons (EA9).

We agree with appellants that none of Sakamoto, Wong '643,
or Wong IEEE discloses or suggests comparing two DC simulation
results performed at the beginning and end of a functional cycle

and then performing manual corrections before carrying out a transient analysis. The examiner has not pointed out where each step is found in the references. Thus, the rejection does not establish a prima facie case of obviousness. The rejection of claims 1, 2, 5-8, 13, and 14 is reversed.

<div align="center">CONCLUSION</div>

The rejections of claims 1, 2, 5-8, 13, and 14 are reversed.

<div align="center">REVERSED</div>

LEE E. BARRETT   )
Administrative Patent Judge   )
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)   BOARD OF PATENT
JAMESON LEE   )   APPEALS
Administrative Patent Judge   )   AND
)   INTERFERENCES
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SALLY C. MEDLEY   )
Administrative Patent Judge   )
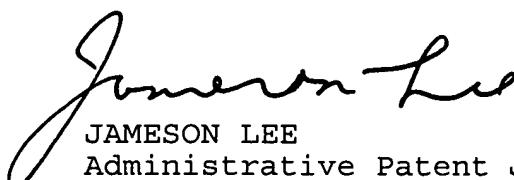
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